Design and Simulation of a 4H-SiC Low Gain Avalanche Diode with Trench-Isolation

Sebastian Onder[a,*], Philipp Gaggl[a,*], Jürgen Burin[a], Andreas Gsponer[a], Matthias Knopf[b], Simon Waid[a], Neil Moffat[c], Giulio Pellegrini[c], Thomas Bergauer[a]

[a] *Institute for High Energy Physics, Austrian Academy of Sciences, Nikolsdorfer Gasse 18, 1050, Vienna, Austria*
[b] *Atominstitut, TU Wien, Stadionallee 2, 1020, Vienna, Austria*
[c] *Instituto de Microelectronica de Barcelona, IMB-CNM-CSIC, 08193, Barcelona, Spain*

Abstract

We present the design and simulation of a 30 µm thick 4H-SiC Low Gain Avalanche Diode (LGAD) optimized for high-voltage operation. A 2.4 µm thick epitaxially grown gain layer enables controlled internal amplification up to 1 kV reverse bias, while maintaining full depletion below 500 V. Electrical characteristics, including I-V, C-V, and gain behavior, were simulated in Synopsys Sentaurus Technology Computer-Aided Design (TCAD) using a quasi-1D geometry and verified across process-related variations in gain layer parameters. To ensure high-voltage stability and proper edge termination, a guard structure combining deep etched trenches and deep p^+ junction termination extension (JTE) implants was designed. TCAD simulations varying the guard structure dimensions yielded an optimized design with a breakdown voltage above 2.4 kV. A corresponding wafer run is currently processed at IMB-CNM, Barcelona.

Keywords: high-energy physics, particle detector, silicon carbide, low gain avalanche diode, LGAD, TCAD

1. Introduction

The growing demand for silicon carbide (SiC) devices in the power electronics and automotive industry has improved both the material's availability and fabrication techniques. This progress has renewed interest in using SiC, especially its prominent polytype 4H-SiC, as a base material for radiation sensors [1, 2, 3]. Due to its significantly larger bandgap compared to the commonly used silicon (Si), 4H-SiC exhibits low dark current levels (< 10 pA), even after irradiation and at room temperature [4, 5]. Its high breakdown field and charge carrier saturation velocity enable fast signal generation and operation at considerably high reverse bias, which could be leveraged for fast timing detectors in high-energy physics (HEP).

However, current epitaxial growth techniques commonly used within industry yield relatively high doping concentrations ($\geq 10^{14}$ cm^{-3}). The subsequently large depletion voltages render thicker active regions impractical due to challenges regarding high-voltage stability. This currently limits SiC particle detectors to active thicknesses of around 100 µm [2]. Furthermore, 4H-SiC has a higher electron-hole pair creation energy than Si (Si: 3.6 eV, 4H-SiC: $\sim$ 7.8 eV). A minimum ionizing particle (MIP) only generates about 57 electron-hole pairs per µm in SiC, roughly two-thirds relative to Si [6]. Conventional SiC pn-junction sensors thus only yield small signal amplitudes that are insufficient to detect MIPs, gravely limiting the attractiveness of the material for the HEP community.

In contrast, Si-based low gain avalanche diodes (LGADs) have been successfully used in HEP experiments as fast timing detectors by taking advantage of an additional highly doped gain layer, enabling internal signal amplification due to charge multiplication [7]. Successfully realizing such a design using 4H-SiC potentially compensates for the inherently small signals in conventional SiC sensors. Considering its naturally fast signal generation and a low dark current, 4H-SiC is an ideal candidate for LGAD development and detectors with ultra-fast timing performance. Several groups have already demonstrated prototype SiC-LGADs. The SICAR project designed devices using a bevel-edge process for isolation, reporting a gain of 2-3 [8]. A production from LBNL and NCSU used a similar isolation approach, reporting a gain of 7-8 and time resolution of < 35 ps based on UV-TCT measurements [9]. The latest production of 4H-SiC LGADs from FNSPE CTU and FZU CAS in collaboration with ON Semiconductor [10] used implanted junction termination extensions (JTEs) for isolation and managed to reach an epitaxial layer doping down to 5×10^{13} cm^{-3}. They reported a gain of 10-100.

We present a TCAD-based design of a 4H-SiC LGAD, featuring trench isolation combined with deep-implanted JTEs optimized for high-voltage operation. A corresponding wafer run has already been fabricated and received, while several processing steps, such as metallization and trench etching, remain pending at IMB-CNM in Barcelona, Spain [11].

2. Device Design

2.1. Epitaxial Structure

Fig.1 shows a cross-section of the epitaxial structure for the proposed 4H-SiC LGAD design. The device is grown on a

*corresponding author
Email addresses: `sebastian.onder@oeaw.ac.at` (Sebastian Onder), `philipp.gaggl@oeaw.ac.at` (Philipp Gaggl)

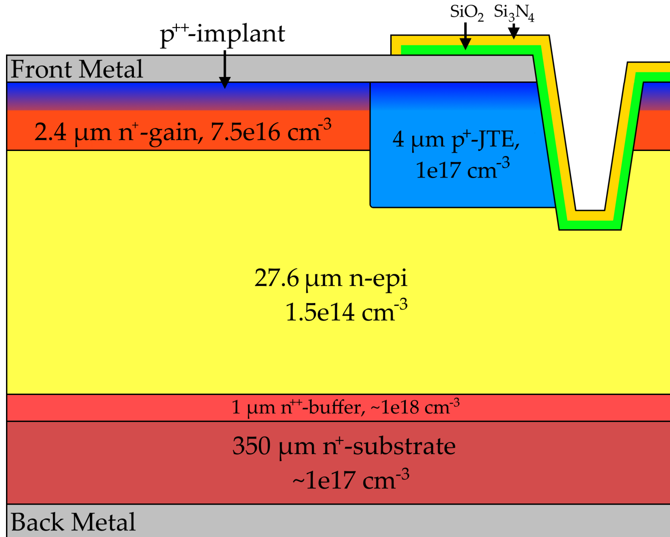


Figure 1: Cross-section of the epitaxial structure of the 4H-SiC LGAD design (not true to scale). The edge of the front contact and the subsequent guard structure are shown. The latter consists of an etched trench and a JTE implant to further distribute fringe fields.

low-quality n^+ substrate with a doping concentration of approximately $10^{17}\,\mathrm{cm}^{-3}$. On top, a 1 µm thick, highly doped ($\sim 10^{18}\,\mathrm{cm}^{-3}$), n^{++} buffer layer serves as a field stop. The active region consists of a highly resistive, 27.6 µm thick, n-type epitaxial layer with a doping concentration of $1.5 \times 10^{14}\,\mathrm{cm}^{-3}$, followed by a 2.4 µm n^+ gain layer with a doping of $7.5 \times 10^{16}\,\mathrm{cm}^{-3}$. Finally, a p^{++} implant establishes the pn-junction, while simultaneously providing an ohmic contact to the front metallization.

As the excessively high implantation energies required to implant sufficiently deep (≈ 1 µm) were not available to us, an epitaxial growth step was utilized to deposit the gain layer across the entire wafer. To that end, a non-buried approach was chosen to eliminate the potential risk of residual doping of unknown intensity subsequent to the gain layer. The above-reported gain layer thickness thus spans from the very top of the device, even though parts of it are compensated by the p^{++}-implant. The doping concentration of the n-epi layer represents the lowest possible concentration the manufacturer could reliably provide, aiming to minimize the full depletion voltage. The device thickness, as well as the thickness and doping concentration of the gain layer, were optimized through extensive parameter sweeps in Synopsys Sentaurus TCAD [12]. The target requirements included a full depletion voltage below 500 V, stable operation up to 1 kV reverse bias, and a signal gain (when compared to a common PIN diode of equal thickness) between 2 and 10.

Ten wafers with the finalized structure have been manufactured and received. According to the manufacturer, the gain layer has a thickness tolerance of 0.2 µm and a doping variation of up to 10 %, which justifies the decision to utilize a relatively thick gain layer with moderate doping, ensuring robustness against such uncertainties.

2.2. Guard Design

Because the gain layer is grown homogeneously across the full 4H-SiC wafer and has a relatively large thickness, conventional guard structures using shallow p-implants are insufficient to isolate and shield individual LGADs properly. To ensure reliable edge termination, the design incorporates etched trenches surpassing the gain layer thickness, as shown in Fig.1. These trenches, soon to be processed at IMB-CNM, are unfilled and passivated along the walls via deposition of a SiO_2/Si_3N_4 stack. The trenches enclose the entire active area of the circular diodes with a diameter of 500 µm.

Initial simulations of the trench geometry, including trench width, depth, angle, and potential etching edges, revealed the trench angle to play a critical role in breakdown behavior. Specifically, trench wall angles exceeding 90° (relative to the wafer surface) accumulate a high electric field at the inner trench corner located on the surface of the substrate, provoking premature breakdown below 1 kV reverse bias. To mitigate this, an additional p^+ JTE was introduced at the inner side of the trench. Early simulations incorporating shallow JTE implants (not surpassing the gain layer), as fabricable at IMB-CNM, already showed notable improvements, with breakdown voltages rising above 1 kV. However, through a collaboration with mi2-factory [13], sufficiently high implantation energies to penetrate the gain layer (up to 4 µm) became accessible. Introducing such deep JTEs with an implant depth of 4 µm and a uniform doping concentration around $10^{17}\,\mathrm{cm}^{-3}$ into the model significantly improved breakdown stability by relocating electric field peaks into lower doped regions. Such a design also covers potential uncertainties in manufacturing, as simulations only suggest a slight dependence of the breakdown voltage on trench angle and potential etching edges. Guard structure design parameters were optimized via TCAD breakdown simulations, details of which are presented in section 3.3. The final design parameters are summarized in Tab.1.

	width (µm)	depth (µm)	doping (cm^{-3})
trench	5/10/15*	7	-
JTE	30	4	10^{17}

Table 1: Optimized guard structure design parameters according to performed TCAD breakdown simulations. *Value confined by the manufacturer, despite simulations suggesting better performance at larger widths (see section 3.3).

3. Simulation

The simulation results presented in the following were obtained using Sentaurus TCAD SDevice. We evaluated the current (I-V), capacitance (C-V), and signal gain characteristics as a function of the applied reverse bias to reach the LGAD design presented in section 2.1. These simulations, as described in section 3.1.1, contained a wide range of design parameters and considered manufacturing tolerances as given by the vendor. Any fringe structures, such as the guarding, however, were omitted due to their negligible effect on the relevant simulation output. After finalizing the LGAD design, additional simulations incorporating a variety of guard structures were carried

out (section 3.1.2). In all cases, the gain layer was implemented via a box profile and according to specifications given in section 2.1. Any simulated metallization used titanium as electrode material.

3.1. Simulation Setup and Method

3.1.1. Gain Layer Design

To reduce computation time, the simulations of I-V, C-V, and gain characteristics utilized a quasi-1D geometry of 1 μm width, omitting any edge structures. Apart from the low-quality substrate, the full vertical epitaxial stack shown in Fig.1 was considered. The low structure complexity allowed for extensive meshing along the vertical (depth) axis to accurately resolve doping profiles and subsequently emerging potentials. Laterally, four grid lines were used in order to avoid encountered bugs with the *HeavyIon* model, utilized to model transient signal response to particle hits. To determine the signal gain, a conventional PIN diode identical to the LGAD model, but omitting the gain layer, was simulated to serve as reference.

I-V and C-V characteristics were obtained simultaneously using quasistationary voltage ramps up to 1 kV reverse bias, and contained a termination option in case current levels exceeded device breakdown. Capacitance behavior was determined via a *Mixed-Mode* AC simulation at 10 kHz. The resulting potentials and electric fields were saved every 10 V, and later used as input for transient signal simulations. To evaluate the signal response to a particle hit, transient simulations were performed using the *HeavyIon* model, emulating a MIP. A linear energy transfer (LET) factor of 9.15 pC μm^{-1}, gaussian lateral width of 0.15 μm, and temporal width of 0.5 ps were chosen within the *HeavyIon* parameter set, to reproduce a realistic charge deposition of 57 electron-hole pairs per μm, the most probable value for 4H-SiC [6]. The signal gain was then calculated by normalizing the integrated current signal from the respective LGAD structure to that of the reference PIN diode.

Due to the low intrinsic carrier concentration in 4H-SiC, all simulations required adapted convergence, error, and solver settings to prevent convergence issues [14]. An artificial carrier generation rate using the *ConstantCarrierGeneration* statement was applied to emulate an electronic noise baseline of approximately 1 pA, consistent with measured data from reference samples [4, 5]. The *Okuto* impact ionization parameter set was used to model charge multiplication. Anisotropy was considered using a conventional cutoff angle of 4°. For further details on the physical models and custom 4H-SiC material parameters used in the simulations, as well as tightened error and convergence criteria, see [14, 15].

3.1.2. Guard design

The breakdown behavior of the finalized LGAD design was investigated via 2D simulations, incorporating the full vertical epitaxial layer stack as described previously. To reduce computation time, the simulated geometry was limited to the immediate vicinity of the guard structures, i.e., the JTE implant and the trench. As such, only a small part (15 μm) of the pad contact was included in the simulation. The distance between the outer boundary and the end of the guard structure was chosen such that no residual electric field was present at the boundary during breakdown, allowing for full propagation of all emerging fringe fields. The vertical doping profile for a 4 μm deep JTE implant was provided by mi2-factory. The passivation was modeled as a 700 nm thick SiO_2, and a 500 nm thick Si_3N_4 layer, consistent with manufacturing specifications. Passivation openings at the pad contact are according to the design rules given by IMB-CNM.

Preliminary simulations indicated a trench wall angle deviating from 90° to have negligible influence on the breakdown voltage, as long as the JTE implants surpassed the gain layer. Therefore, a constant sidewall angle of 96°, taken from preliminary etching tests on 4H-SiC bulk wafers by IMB-CNM, was assumed for all subsequent simulations. The meshing procedure was adapted to the local complexity of the structure, yielding a moderately fine mesh within the gain and passivation layers, and a very fine mesh at critical regions such as material interfaces, doping transitions, and corners of the trench and JTE implant.

Breakdown voltages were extracted using quasistationary simulations with a reverse bias ramp. A current value that could reliably be attributed to device breakdown was obtained through test simulations and used as a termination trigger for all simulations. The breakdown voltage was then determined as the last voltage simulated at termination. A parametric sweep of JTE width, trench width, and trench depth was performed to identify the most stable configuration under high-voltage operation. All material parameters, physical models, and error and convergence criteria were kept identical to the simulations described in section 3.1.1. For the passivation layers, default material parameters provided by Sentaurus TCAD were used.

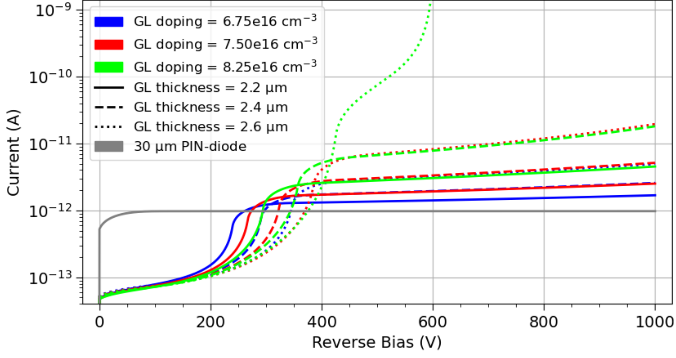
3.2. I-V, C-V and Gain Characteristics

Fig.2 a and b show the simulated I-V and C^{-2}-V characteristics of the proposed LGAD design in comparison to a 30 μm thick PIN diode without gain layer. Results are also shown for potential variations in the gain layer thickness (±0.2 μm) and doping concentration (±10 %) as reported by the manufacturer. A breakdown in the gain layer is only observed for the case with both maximum thickness and highest doping concentration. For all other configurations, the gain layer depletes at voltages below 400 V, with full device depletion occurring below 500 V, and dark current levels remaining under 30 pA.

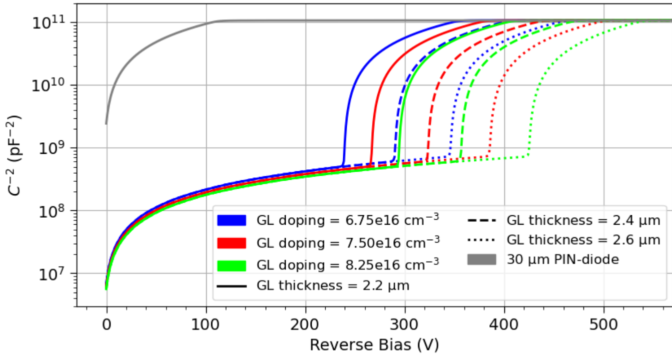
Fig.3 depicts the simulated gain as a function of the applied reverse bias across the same range of gain layer variations. Excluding the single breakdown case identified above, the gain increase with reverse bias is rather smooth, while exhibiting a slightly steeper slope for thicker/more heavily doped gain layers, as one would expect. The simulations predict a signal gain in the range of approximately 1 to 10, indicating a stable amplification behavior within the expected parameter window.

3.3. Breakdown Behavior

Using the simulation geometry described in section 3.1.2, the breakdown behavior of the LGAD design was simulated for



(a) I-V



(b) C-V

Figure 2: Simulated I-V and C^{-2}-V characteristics of a 4H-SiC LGAD without guarding structures compared to a 30 µm thick PIN diode.

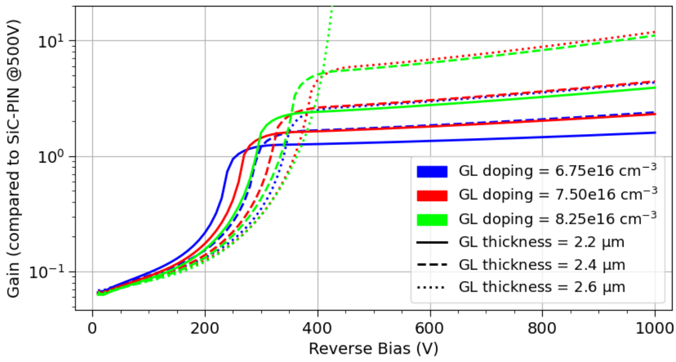


Figure 3: Simulated gain of a 4H-SiC LGAD without guarding structures, as a function of the applied reverse bias. Values are determined by comparing the respective integrated current pulse generated by a MIP in the LGAD structure to that of a 30 µm PIN diode at 500 V bias.

varying JTE implant widths, trench widths, and trench depths. A sweep over JTE widths revealed a clear saturation of the breakdown voltage beyond a width of 30 µm, independent of the trench dimensions. This value was, therefore, selected as the JTE width for the final design. Fig.4 shows a heatmap of the simulated breakdown voltages for all considered combinations of trench widths and depths. While breakdown voltages above 1 kV could be achieved across all configurations, the trench width showed a more pronounced impact on performance than the depth, which displayed a non-monotonic trend: The shallowest depth of 5 µm resulted in the earliest breakdown. Increasing the depth initially improved performance. But, for depths beyond 7 µm, a gradual decline in breakdown voltage was observed. The optimal trench depth was therefore found to be 7 µm. In contrast, the trench width consistently improved the breakdown voltage across the simulated range. The best performance was achieved at the largest trench width of 16 µm. Combined with the optimal JTE width and trench depth, a maximum breakdown voltage of 2450 V could be obtained, demonstrating more than sufficient high-voltage stability. However, the final design, as given in Tab.1, only features narrower variations of trenches. This is a result of restrictions by the manufacturer, as wider trenches inhibit larger risks of large-area surface damage during etching.

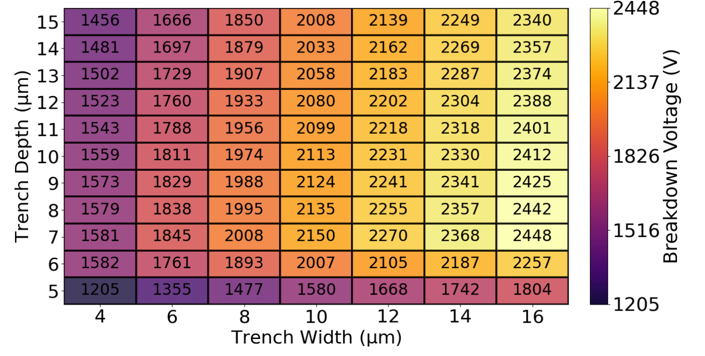


Figure 4: Breakdown voltage of the SiC LGAD design versus trench width and depth for a fixed *p*+-JTE implant with a width and depth of 30 µm × 4 µm.

4. Summary

In this work, we presented the design and simulation process of a 30 µm thick 4H-SiC LGAD structure with trench isolation optimized for high-voltage stability. The 2.4 µm thick gain layer was realized through epitaxial growth rather than implantation, enabling a homogeneously doped profile that allows for full depletion below 500 V. Key electrical characteristics, including I-V, C-V, and signal gain behavior, were simulated using a simplified quasi-1D device geometry, accounting for fabrication tolerances reported by the manufacturer.

To ensure robust edge termination, a guard structure employing 7 µm deep etched trenches was designed. For additional high-voltage stability, high-energy implanted p^+ JTEs with width and depth of 30 µm × 4 µm and a doping concentration of 1×10^{17} cm^{-3} were integrated adjacent to the trenches. A parametric sweep over trench and implant dimensions identified the reported optimal configuration, achieving a suggested simulated breakdown voltage exceeding 2.4 kV. Fabrication of the final design is currently underway at IMB-CNM in Barcelona.

Acknowledgements

This work was supported by the Austrian Research Promotion Agency (FFG) in the project "HiBPM" (883652), by the Spanish Ministry of Science, Innovation and Universities (grant number CEX2023-001397-M), and by the European Union's

ERDF program (MCIN/AEI/10.13039/501100011033/) “A way of making Europe” under grant reference PID2021-124660OB-C22.

References

[1] F. Nava, et al., Silicon carbide and its use as a radiation detector material, Measurement Science and Technology 19 (10) (2008) 102001. doi:10.1088/0957-0233/19/10/102001.

[2] M. De Napoli, SiC detectors: A review on the use of silicon carbide as radiation detection material, Frontiers in Physics 10 (2022) 898833. doi:10.3389/fphy.2022.898833.

[3] I. Capan, 4H-SiC Schottky Barrier Diodes as Radiation Detectors: A Review, Electronics 11 (4) (2022) 532. doi:10.3390/electronics11040532.

[4] P. Gaggl, et al., Charge collection efficiency study on neutron-irradiated planar silicon carbide diodes via UV-TCT, NIM-A 1040 (2022). doi:10.1016/j.nima.2022.167218.

[5] A. Gsponer, et al., Neutron radiation induced effects in 4H-SiC PiN diodes, JINST 18 (11) (nov 2023). doi:10.1088/1748-0221/18/11/C11027.

[6] M. Christanell, et al., 4H-Silicon Carbide as particle detector for high-intensity ion beams, JINST 17 (01) (2022). doi:10.1088/1748-0221/17/01/c01060.

[7] G. Pellegrini, et al., Technology developments and first measurements of Low Gain Avalanche Detectors (LGAD) for high energy physics applications, NIM-A 765 (2014) 12–16. doi:10.1016/j.nima.2014.06.008.

[8] S. Zhao, et al., Electrical Properties and Gain Performance of 4H-SiC LGAD (SICAR), IEEE Transactions on Nuclear Science 71 (11) (2024) 2417–2421. doi:10.1109/TNS.2024.3471863.

[9] T. Yang, et al., Ultra-Fast 4H-SiC LGAD with Etched Termination and Field Plate, IEEE Electron Device Letters (2025) 1–1doi:10.1109/LED.2025.3548509.

[10] R. Novotný, et al., First generation 4H-SiC LGAD production and its performance evaluation, arXiv preprint (2025). doi:10.48550/arXiv.2503.07490.

[11] IMB-CNM (Centro Nacional de Micróelectronica)-CSIC (2024). [link]. URL http://www.cnm.es/

[12] Synopsys Sentaurus TCAD Ver. V-2023.09, Synopsys, Inc., Mountain View, CA, USA., https://www.synopsys.com (2025).

[13] mi2-factory GmbH, Jena, Germany, https://mi2-factory.com/ (2025).

[14] P. Gaggl, Improving TCAD simulation of 4H silicon carbide particle detectors presented at 42nd RD50 workshop, Tivat, Montenegro, https://indico.cern.ch/event/1270076/contributions/5450202/ (Jun 2023).

[15] P. Gaggl, TCAD simulations of 4H-SiC LGADs presented at 43rd RD50 workshop, CERN, Switzerland, https://indico.cern.ch/event/1334364/contributions/5672054/ (Nov 2023).