Simulation-Based Approaches for Comprehensive Schmitt-Trigger Analyses

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***Abstract*— Schmitt-Triggers (S/Ts) are often utilized to clean noisy analog signals at intermediate voltage values in digital circuits. However, they are vulnerable to metastability, which may cause the same undesired non-digital output behavior that was supposed to be removed in the first place. To enable an efficient characterization of static and dynamic metastability properties of S/Ts (e.g., the metastable voltages, the resolution time constants and the overall total resolution times), this work introduces multiple simulation approaches based on control theory, AC, DC and transient analyses. The accuracy and runtime of all methods are compared and discussed by applying them to an analytically describable idealized circuit model as well as three common circuit implementations. Altogether, this work represents a comprehensive resource for investigating the metastable behavior in S/Ts. Even more, the proposed methods are applicable beyond the S/T, enabling an efficient characterization of static and dynamic metastable behavior in general circuits as well.**

***Index Terms*— Schmitt-trigger, metastability characterization, instability analysis, metastable states.**

I. Introduction

In digital circuits, information is carried by binary logic signals, which are considered `HI` if the analog voltage is close to V_{DD}, and `LO` when it is close to *GND*. Any intermediate voltage levels must be avoided, as they impair the performance of digital circuits in terms of logic behavior and timing. In this context, an S/T is crucial to establish signal integrity by converting any undecided or noisy input voltage into a clean and stable binary logic signal [1]. It therefore applies a higher threshold for rising input transitions (V_H) than for falling ones (V_L), which forms a hysteresis in the input/output behavior, see Fig. 1. This, however, implies that the S/T has to be considered as stateful element that, inevitably, suffers from metastability [2]. Due to its wide range of application, e.g., among others for reliable circuits [3], oscillators [4] or SRAM [5], a comprehensive analysis of its static and dynamic metastability properties is therefore key to robust and optimized digital circuit design.

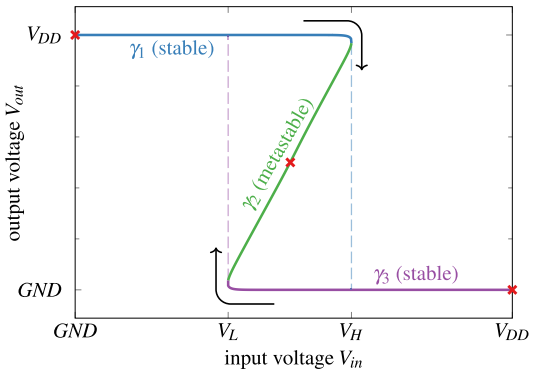

Fig. 1. (Meta)Stable states of a latch (×) and an S/T (lines) forming the characteristic z-shaped curve.

S/Ts substantially differ from latches, which are well researched in the literature (see Section II). While latches exhibit only a single metastable state, the input of S/Ts remains connected all the time, which gives rise for a whole range of metastable voltages $V_M(V_{in})$. Previous works investigated the metastable states and dynamics of S/Ts based on analytical models [6]–[9], detailed SPICE simulations [1], [10] and experimental measurements [11], [12]. However, efficient methods that facilitate a quantification of the metastability behavior in practice, have, to the best of the authors' knowledge, not been published.

Contribution: This work presents a set of methods that, utilizing analog *HSPICE* simulations, enable a comprehensive characterization of metastability in S/Ts. In detail, static (metastable voltages) and dynamic (resolution time (constant)) properties are determined using control theory, AC, DC and transient analyses. All presented approaches are verified against the analytic results of [6] as ground truth, applied to modern transistor level circuit implementations and evaluated against each other. In summary, we believe that this publication can serve as a self-contained resource for metastability analyses of S/Ts, whereat each approach can be easily adapted to the specific implementation at hand.

This work is organized as follows: In Section II we briefly review the metastability properties of S/Ts. Next, Section III presents methods for obtaining a first overview of the S/T characteristics. In Sections IV and V follows a description of the proposed precise characterization methods for static respectively dynamic parameters. Results for three common implementations are discussed in Section VI, which is followed

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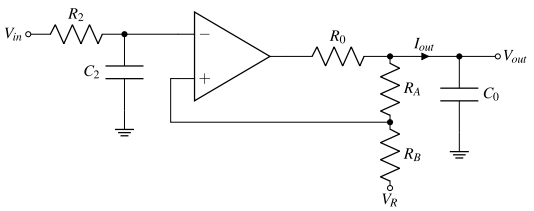


Fig. 2. Schmitt-Trigger implementation studied in [6].

by a comparison and evaluation of the presented methods in Section VII. Finally, Section VIII concludes this paper and gives an outlook to future research directions.

II. Background

For latches, which are formed by cross-coupled inverters, metastability has been well researched, whereat the main results are published in the seminal work by Kinniment and Edwards [13], Chaney and Molnar [14], and Veendrick [15]. In hold mode the inverter loop is decoupled from the input. Consequently, it solely has two stable and one metastable state (see Fig. 1; V_{in} and V_{out} represent the node voltages in the loop). The resulting simplicity even allows to derive an expression for the mean time between metastable upsets (MTBU) [16] which relies, besides others, on the metastable resolution time constant τ_C.

Unfortunately the situation is much more complicated for S/Ts since the input remains connected at all times and hence has to be considered as well. For this purpose, Marino [6] modeled the S/T by a properly wired operational amplifier (OpAmp), see Fig. 2, and carried out analytic considerations. He determined the phase diagram V'_{out} over the V_{in}-V_{out} plane, as shown in Fig. 3, where A denotes the amplifier gain and M the output saturation voltage. This way, the behavior is divided into three distinct regions. The output voltage V_{out} in each region is governed by the following equations:

$$\text{Region 1: } \frac{\mathrm{d}V_{out}}{\mathrm{d}t} = V'_{out} = -\frac{1}{\tau_1}(V_{out} - \gamma_1) \tag{1}$$

$$\text{Region 2: } \frac{\mathrm{d}V_{out}}{\mathrm{d}t} = V'_{out} = +\frac{1}{\tau_2}(V_{out} - \gamma_2) \tag{2}$$

$$\text{Region 3: } \frac{\mathrm{d}V_{out}}{\mathrm{d}t} = V'_{out} = -\frac{1}{\tau_3}(V_{out} - \gamma_3) \tag{3}$$

For Regions 1 and 3, V_{out} is described by decaying exponential functions (time constant $\tau_1 = \tau_3 \approx R_0 C_0$) which asymptotically approach the truly stable rest points $\gamma_1 \approx M$ and $\gamma_3 \approx -M$, respectively. For Region 2 V_{out} moves away from the metastable rest point $\gamma_2 \approx \frac{V_{in}-(1-k)V_R}{k-1/A}$ in an exponentially growing fashion with time constant $\tau_2 \approx \frac{R_0 C_0}{kA-1}$. Note the dependence of γ_2 on the input voltage V_{in}. This implies that the S/T has infinitely many (meta-)stable values which range continuously from the lower (*GND*) to the upper (V_{DD}) supply voltage. As shown in [1] a malicious input signal, i.e., exceeding the threshold and then steering back, is able to reach any of these values and hold them forever.

The phase diagram as proposed by Marino can be understood as a finger print of an S/T implementation which helps the designer to comprehend and optimize the circuit. While the stable states on γ_1 and γ_3 are easily determined, the task to identify γ_2 is much harder. In this paper we thus present multiple approaches to determine the static and dynamic metastability parameters of an S/T. Since analytic evaluations of abstract models lack accuracy, especially for modern technologies, our analyses are based entirely on analog simulations in *HSPICE* (version 2018.09). To this end we use a 28 nm technology library with a supply voltage of $V_{DD} = 0.9\,\mathrm{V}$. Comparisons with an older 65 nm UMC technology showed no qualitative difference and therefore we settled to presenting solely the former in this paper.

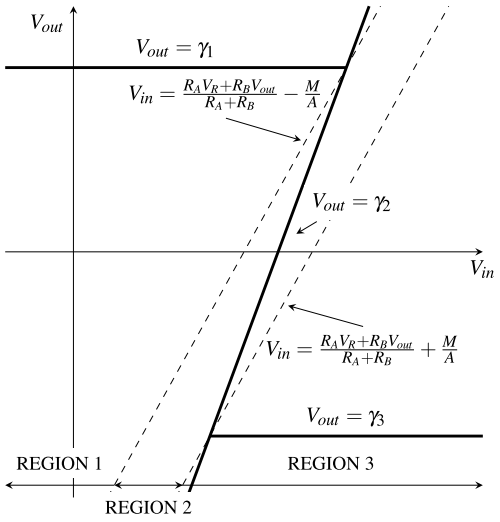


Fig. 3. Phase diagram of the S/T [6].

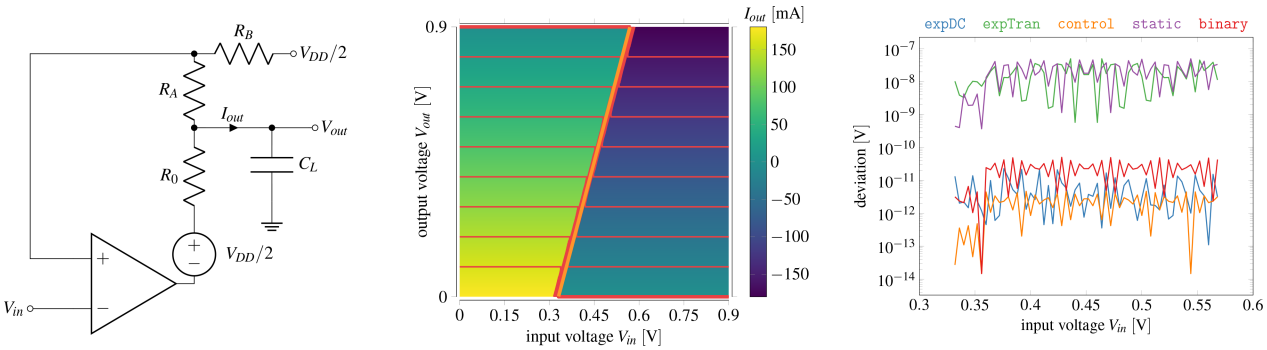
III. Obtaining an Overview

In this section, we present a number of approaches to characterize the overall properties of an S/T implementation. The subsequent Sections IV and V then introduce specific methods to precisely characterize the metastable states γ_2 and the resolution behavior.

In order to explain and evaluate our approaches, we first apply them to the circuit `opamp` shown in Fig. 4a, which is a slightly modified version of Marino's idealized model implementation (cf. Fig. 2). This allows a simple accuracy assessment of the respective methods, as an analytical ground truth can be obtained from theory. Since Marino's parametrization leads to a close to ideal behavior with a narrow Region 2, which is hardly comparable to real-world circuits, we chose $A = 50$ and $C_L = 10\,\mathrm{pF}$ to obtain a more realistic behavior. Furthermore, the parameters $R_A = 10\,\mathrm{M\Omega}$, $R_B = 4\,\mathrm{M\Omega}$, and $R_0 = 5\,\Omega$ keep the voltage drop across R_0 at a low level. Finally, note that we added an offset of $V_{DD}/2$ at the output of the OpAmp and chose $V_R = V_{DD}/2$ since our tool was designed for the voltage range $[0, V_{DD}]$.

A. Hysteresis (`hyst`)

The stable states on γ_1 and γ_3 can be easily obtained by starting two *DC* analyses, one sweeping V_{in} from *GND* to V_{DD} and one in the opposite direction. From the results, the threshold voltages V_L and V_H can be identified in a straight forward manner: Exceeding the relevant threshold value on V_{in} leads to a major jump on the corresponding stable value V_{out}. For the circuit `opamp` we get $V_H = 570\,\mathrm{mV}$ and $V_L = 330\,\mathrm{mV}$, which is in perfect agreement to analytic evaluations.



(a) transistor level implementation (b) I_{out} by `map` (c) V_M predictions vs. theory

Fig. 4. Metastability simulation results for `opamp`.

B. Exponential Voltage Trajectories

Marino already showed that V_{out}, and thus in consequence also V'_{out}, evolves exponentially over time in all regions, albeit with different time constants: In Regions 1 and 3 the values of τ_1 and τ_3, respectively, are constituted[1] by $R_0 C_L$, while in Region 2 the activity of the non-saturated operational amplifier reduces τ_2 by a factor of $\frac{1}{kA-1}$ with $k = \frac{R_B}{R_A+R_B+R_0}$.

This exponential trend can be verified by depicting V_{out} and V'_{out} in a semi-logarithmic plot over time – which, within one region, yields a perfectly straight line for the `opamp` case. In this work, the resolution trajectories of V_{out} that start within Region 2 and are described in (2) are of specific interest. The solution of the differential equation is an exponentially growing function of the shape

$$V_{out} = V_M \pm V_x \exp\left(\frac{t-\widehat{t}}{\tau}\right) \tag{4}$$

$$V'_{out} = \pm\frac{1}{\tau} V_x \exp\left(\frac{t-\widehat{t}}{\tau}\right), \tag{5}$$

where $\widehat{t}$ denotes the unknown time shift, $V_x > 0$ the unknown scaling factor of the exponential function and τ a general time constant. The fact that V_x and $\widehat{t}$ could be easily combined into a single parameter shows that multiplying an exponential with a constant is equivalent to a time shift. In consequence, the signal shape and especially the derivative remain unchanged in any arbitrary point V_1 on the function. In other words, the trajectory is independent of whether the voltage value V_1 represents the (static) starting point or is (dynamically) "passed by". This is a specific property of a first-order system that becomes invalid for higher order ones.

For $\lim_{t\to-\infty}$, the time evolution expressed in (4) asymptotically approaches the metastable voltage V_M, i.e., the value of interest. More precisely, $V_M(V_{in})$ is a function of the input voltage and essentially corresponds to Marino's γ_2. To remain consistent, we will use γ_2 to refer to the whole function, while V_M denotes the one metastable voltage for a specific V_{in}.

The resolution behavior in the form of exponentially growing trajectories has major implications. Firstly, it suggests a behavior comparable to the flip-flop, with the main difference that the metastable voltage V_M is not unique but varies with V_{in}. Secondly, it gives us the possibility to infer the metastable voltage V_M by recording just a short piece of the resolution trajectory and matching the parameters, as will be leveraged in Sections IV-B and IV-C. Thirdly, it is possible to observe a common time constant τ within Region 2. While this is perfectly valid for `opamp`, it will become apparent in real-world circuits (see Section VI) that also τ varies with V_{in} – which makes the exponential description less ideal as well.

[1]In detail, the effective R is the parallel resistance of R_0 and $R_A + R_B$.

C. Voltage Derivative and Current

(Meta)stable states can be uniquely identified by verifying $V'_{out} = 0$; all points on γ_1, γ_2 and γ_3 share this property, cf. (1)–(3). This trivially follows from the fact that perfect (meta)stability demands no change of V_{out} over time. For the circuit `opamp`, V_{out} denotes the voltage drop across the parasitic load capacitance C_L at the output, whose voltage and current follow the well known relation $I_C = C\, V'_C$. Thus we obtain a direct proportionality between I_{out} and V'_{out} as

$$I_{out} = C_L\, V'_{out}. \tag{6}$$

Consequently, the current flowing into C_L, i.e., I_{out} in Fig. 4a, has to vanish in the (meta)stable state. For real circuits (see Section VI) this relationship is more complicated, since these circuits constitute higher-order dynamic systems.

D. Phase Diagram (`map`)

Without prior knowledge, a very pragmatic approach for obtaining the phase diagram is to cover the V_{in}-V_{out} plane with a regular grid and determine V'_{out} for each grid point. Albeit this initially appears quite untargeted and laborious, the resulting phase diagram (denoted as `map`) not only allows to interpolate γ_2, but also provides a good intuition of the overall behavior, especially while resolving metastability.

For determining V'_{out}, the authors in [1] performed a transient analysis for each grid point. In contrast, we opted to use I_{out} and the proportionality (6) between I_{out} and V'_{out} instead. To derive values for the current, a constant voltage source is attached in parallel to the output capacitance. Its value V_{out} is chosen according to the investigated grid point. In the steady state, this forces the current to/from the capacitance to vanish since $V'_{out} = 0$. Instead, I_{out} is flowing through the voltage source, where it can easily be recorded. The respective values can then be used to indicate how fast C_L would be (dis)charged

```
.DC vIn 0 supp width SWEEP vOut LIN count 0 supp
.PROBE DC I(vOut)
```

Listing 1. Deriving I_{out} in V_{in}-V_{out} plane in *HSPICE*.

(resulting in a corresponding V'_{out}), once the voltage source is disconnected.

This approach is considerably faster and much simpler to execute, while providing the same level of accuracy for the metastable voltage.[2] The required simulations are run using built-in commands from *HSPICE*, as detailed in Listing 1: V_{in} is swept from *GND* (0) to V_{DD} (*supp*) in steps (*width*) corresponding to the grid spacing. For each value V_{in} of the input voltage, V_{out} is varied in the same fashion where the number of steps (*count*) can be different. The current through the voltage source V_{out} is determined in the second code line.

Most certainly we won't be fortunate enough to exactly hit $I_{out} = 0$ (or equivalently $V'_{out} = 0$) this way. Nevertheless, γ_2 can already be confined between two adjacent grid points with changing sign. In a first step, contour plots can be used to show (interpolated) lines for constant output current. Especially interesting is $I_{out} = 0$, which corresponds to the (meta)stable states. Overall, `map` provides the possibility to quickly identify the most important parameters of an S/T implementation (e.g., threshold voltages, (meta)stable values, gradients of V'_{out}) and thus to coarsely predict the overall behavior.

The obtained results for the circuit `opamp` shown in Fig. 4b illustrate the very good agreement with the analytic considerations. In particular, horizontal contour lines with linear spacing in Regions 1 and 3, as implied by (1) and (3), are visible. Within a corridor of width $\frac{2M}{A} = 36\,\text{mV}$ around γ_2 the contour lines run parallel to γ_2, in accordance with (2).

IV. Precisely Identifying the Metastable States

The approaches presented so far allow a rough overview of a given S/T implementation, whereat the metastable points constituting γ_2 are obtained by interpolation. In the following, we present a number of methods that allow a more precise description, beginning with a novel method based on control theory termed `control`. Each of them will be applied to the circuit `opamp` for illustration and validation.

A. Closed-Loop Control (`control`)

From a control engineer's perspective, the metastable states of a Schmitt-Trigger are unstable equilibrium points in the state space of a nonlinear time-invariant dynamical system. This becomes evident from the exponential evolution of V_{out} in Section IV-B, see (4). The fact that all trajectories strive to leave these unstable states makes it so hard to obtain the accurate value for the metastable voltage V_M. In the following, we will thus propose the method `control`, which uses a simple proportional controller to stabilize the unstable equilibria. This makes entering metastable states a trivial task.

First, the nonlinear system is characterized as a linear time-invariant (LTI) system in the proximity of a given metastable state using an *AC* analysis in *HSPICE*. Next, the stability boundaries for the controller gain are determined and finally, a suitable controller design strategy is employed to obtain a good closed-loop behavior.

[2]Recall that $V'_{out} = 0$ directly translates to $I_{out} = 0$. Thus considering C_L, including the uncertainties and non-linearities possibly associated with it, is not required.

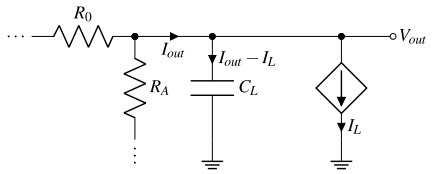


Fig. 5. Circuit setup to characterize the linearized system dynamics and to control (meta-)stable points.

1) Characterization: A circuit is characterized by attaching a current source I_L, which serves as system input for characterization and control, in parallel to the output capacitance C_L. The corresponding setup for the circuit `opamp` is shown in Fig. 5. After initializing the circuit in (or close to) a given metastable state, an *AC* analysis is performed using *HSPICE* to obtain the frequency response of the output current I_{out} resulting from the input current I_L. This way, the circuit is characterized as LTI system with the poles $p_1, \ldots, p_N$ and the zeros $z_1, \ldots, z_M$ of the transfer function

$$G(s) = \frac{I_{out}(s)}{I_L(s)} = -V \frac{(s - z_1)(s - z_2) \cdots (s - z_M)}{(s - p_1)(s - p_2) \cdots (s - p_N)},$$

where $M \leq N$ holds and V normalizes the *DC* gain, i.e., V is determined such that $|G(s)|_{s=0} = 1$. Equivalently, the transfer function $G(s)$ is rewritten as

$$G(s) = \frac{b_M s^M + \ldots + b_1 s^1 + b_0}{a_N s^N + \ldots + a_1 s^1 + a_0} = \frac{n(s)}{d(s)}$$

with $a_N = 1$.

2) Closed-Loop System: The controller $R(s) = K$, which corresponds to a simple proportional controller with the gain K, forms a closed loop together with the system $G(s)$, as shown in Fig. 6. Hence, the control law is implemented simply as $I_L = K\, I_{out}$, in which the controller gain K has to be designed. The closed-loop transfer function $T(s)$ reads

$$\begin{aligned} T(s) &= \frac{R(s)G(s)}{1 + R(s)G(s)} = \frac{K\, n(s)}{d(s) + K\, n(s)} \\ &= \frac{K\, n(s)}{c_N s^N + \ldots + c_1 s + c_0} = \frac{n_T(s)}{d_T(s)}, \end{aligned} \tag{7}$$

with $c_i = a_i + K b_i$ and $b_i = 0$, $i > M$. In Fig. 6, the control input $I_{out,d} = 0$ denotes the desired setpoint value for I_{out}.

3) Stability Boundaries: In the next step, the stability boundaries for the controller gain K in the closed loop are established. The stability of an LTI system is assessed analytically or numerically using the Routh-Hurwitz criterion [17] by examining the denominator polynomial $d_T(s)$ of $T(s)$, see (7). The closed loop is stable if the polynomial $d_T(s)$ is a so-called Hurwitz polynomial of which all roots λ_i, $i = 1, \ldots, N$, lie in the open left half of the complex s-plane, i.e., $\text{Re}(\lambda_i) < 0\ \forall i = 1, \ldots, N$. The necessary condition of the Routh-Hurwitz criterion requires all coefficients of $d_T(s)$ to be non-zero and have the same sign. Hence, the condition

$$(c_i > 0\ \forall i = 0, \ldots, N) \vee (c_i < 0\ \forall i = 0, \ldots, N) \tag{8}$$

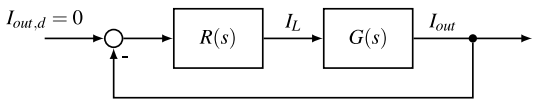


Fig. 6. Closed-loop control with the controller $R(s)$ and the characterized system $G(s)$.

has to be satisfied, which is also a sufficient stability condition for $N \leq 2$. For higher-order systems, the Hurwitz test has to be performed, from which additional (simple) conditions are obtained. For example, testing a polynomial with $N = 3$ leads to the additional condition $c_1 c_2 > c_0$. By combining all conditions from (8) and the additional conditions from the Hurwitz test for $N > 2$, the highest lower bound $\underline{K}$ and the lowest upper bound $\bar{K}$ for the controller gain K are found, i.e., the closed loop is stable for $\underline{K} < K < \bar{K}$.

4) Controller Design: After deriving the gain boundaries $\underline{K}$ and $\bar{K}$, a suitable controller gain K is determined. Two cases have to be distinguished:

a) Case I: If the closed-loop system $T(s)$ exhibits at least one conjugate complex pole pair, it is well approximated by the second-order system

$$T(s) \approx \frac{V\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}, \tag{9}$$

based on the dominant conjugate complex pole pair from (7), which is parametrized by the natural frequency ω_n and the damping $0 \leq \xi < 1$. The most important properties of the approximated system (9) are the rise time t_r and the overshoot o, which read as [17]

$$t_r = \frac{\pi}{2\omega_n\sqrt{1-\xi^2}} \tag{10}$$

$$o = \exp\left(-\xi\pi/\sqrt{1-\xi^2}\right). \tag{11}$$

The design goals for the closed-loop system are a short rise time t_r to reduce transient simulation times in *HSPICE* and low overshoot for fast regulation of the setpoint $I_{out,d}$. However, since these two aspects contradict one another according to (10) and (11), a compromise value of $o = 10\%$ is chosen. Solving (11) for ξ yields the damping $\xi \approx 0.5912$. In order to obtain this damping in the closed-loop behavior, the controller gain K is calculated such that the poles λ of (9) satisfy

$$\left|\frac{\mathrm{Im}(\lambda)}{\mathrm{Re}(\lambda)}\right| = \frac{\sqrt{1-\xi^2}}{\xi} \approx 1.3644. \tag{12}$$

If no solution for (12) exists, the controller gain K closest to this value is chosen using a gradient-free optimization method.

b) Case II: If the closed-loop system $T(s)$ has real poles only, the system response exhibits no oscillations and the control error decays exponentially. In this case, the controller gain is chosen using the simple heuristic formula $K = 1 + 0.9\,(\bar{K} - 1)$. This way, the closed-loop behavior shows fast regulation of the setpoint $I_{out,d}$ and has reasonable robustness w.r.t. uncertainties in the linearized model by employing a 10% margin to the upper stability boundary.

If no upper boundary $\bar{K}$ exists, the closed loop is stable for all $K > \underline{K}$. Higher gain values lead to a lower rise time t_r. While the controller gain K is in theory only bounded from below, also an upper bound exists for the simulation of the full nonlinear model, since the linearized model $G(s)$ is only valid in the proximity of the metastable equilibrium. The closed-loop system might leave this proximity when using high gain values $K \gg \underline{K}$.

```
vMeas out outC DC 0 AC 0 0
cL outC 0 C_L
iL outC 0 DC 0 AC 1 0
.AC DEC 10 1 10000G
.PROBE AC IDB(vMeas) IP(vMeas)
.PZ I(vMeas) iL
```

Listing 2. Circuit characterization for `control` in *HSPICE*

```
vMeas 5 out DC 0
cOut out 0 10p
fP out 0 vMeas K
.MEAS TRAN finalVal FIND V(out) AT=1us
.TRAN 1ns 1us
```

Listing 3. Method `control` in *HSPICE*

5) Closed-Loop Control for Circuit `opamp`: In order to characterize the circuit `opamp`, the *HSPICE* code shown in Listing 2 is used. Over the ideal voltage source *Vmeas* (line 1), which is used to extract I_{out}, the capacitance C_L (line 2) is connected to the circuit. At the same node, the *AC* current source (line 3) introduces the current I_L, which is used as reference in line 5 to calculate gain and phase of I_{out}. Finally in line 6, the poles and zeros are evaluated and exported.

Due to the idealized structure of `opamp`, the characterized LTI system only exhibits a single unstable real pole and its transfer function $G(s)$ is independent from the chosen metastable point, reading as

$$G(s) = \frac{2.6571 \times 10^{11}}{s - 2.6571 \times 10^{11}}. \tag{13}$$

The denominator $d_T(s)$ of the closed-loop transfer function $T(s)$ follows as, see (7), $d_T(s) = s + 2.6571 \times 10^{11}(K-1)$, from which the lower stability boundary $\underline{K} = 1$ is deduced using (8). An upper boundary $\bar{K}$ does not exist and therefore the considerations from Section IV-A.4 (case II) apply.

To obtain the metastable values V_M, transient simulations using Listing 3 are utilized. The controller is implemented as a current control current source (CCCS) (line 3) that multiplies the current through *Vmeas* (line 1), i.e., the current into the artificial capacitance *cOut* (line 2), by the controller gain $K = 2$. The metastable voltage V_M is finally extracted as the value of V_{out} after $1\,\mu$s (line 4).

The achieved results for `opamp` are shown in Fig. 4c. We observe an absolute error of $\approx 1\,$pV compared to the analytic calculations, which is, as we will see later on, among the best. Note that increasing the simulator time steps allowed us to increase the simulation time while maintaining a constant computation time, which in turn leads to more accurate results.

B. Transient Estimation (`expTran`)

In Section III-B we expressed the metastable voltage in (4). In fact by combining (4) and (5), V_M can be determined from a pair of corresponding values V_{out} and V'_{out} as

$$V_M = V_{out} - \tau\, V'_{out}. \tag{14}$$

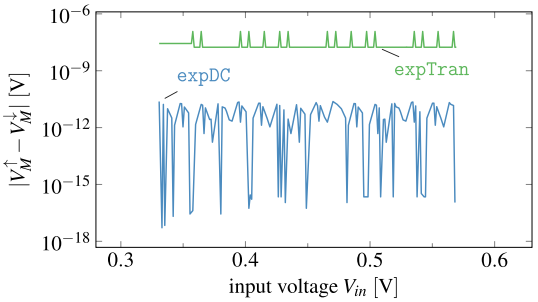


Fig. 7. Absolute deviation between V_M predictions based on the resolution direction.

Note that the unknown V_x and $\widehat{t}$ are eliminated. Consequently, τ is the only remaining parameter, which can be determined by applying the natural logarithm to (5), yielding

$$\ln(|V'_{out}|) = \ln\left[\frac{1}{\tau} V_x \exp\left(-\frac{\widehat{t}}{\tau}\right)\right] + \frac{t}{\tau} = K + \frac{t}{\tau}. \quad (15)$$

Overall we thus obtain the following strategy: From a transient simulation starting in an arbitrary point (V^*_{in}, V^*_{out}), we use the time and value differences among simulated values of V'_{out} to determine τ according to (15). A single consistent pair of $(\widehat{V}_{out}, \widehat{V}'_{out})$ then suffices to obtain V_M from (14). As outlined in Section III-B, the time constant of the exponential function changes as soon as the operational amplifier saturates, i.e., when the trajectory leaves Region 2 and enters Region 1 or 3. Since we are interested in the former, we must take care to stay within Region 2 for the parameter fitting.

Note that `expTran` can be run twice for each input voltage, since resolution traces to *GND* and V_{DD} are possible. Ideally both would render the same results. In reality, however, we get slightly differing values for τ and V_M. These can be retraced to numerical issues due to the limited accuracy of the simulations. Fig. 7 shows the difference between the predictions of V_M for the curve resolving to V_{DD} $(V_M^{\uparrow})$ and *GND* $(V_M^{\downarrow})$ using the method `expTran`. To improve accuracy, we thus determine the intersection point of both linear functions resulting from (14), i.e., one for each direction.

We experienced that the values predicted for the resolution time constant τ are comparably accurate (relative error $\approx 10^{-7}$), but *HSPICE* fails to deliver good values for V'_{out}, which have a relative error of up to 1%. Fortunately, this mismatch can be largely mitigated by a careful choice of $\widehat{V}_{out}$: One way of interpreting (14) is that an initial value $\widehat{V}_{out}$ is corrected by the term $\tau\,\widehat{V}'_{out}$. With a choice of $\widehat{V}_{out}$ close to V_M (in our case $|\widehat{V}_{out} - V_M| \approx 10^{-5}$ V) that correction term becomes small such that a deviation less than 10^{-7} V can be achieved, which is quite big compared to other methods (see Fig. 4c). Increasing the simulator accuracy improves the results, but also leads to a prolonged computation time.

C. Static Estimation (`expDC`)

Eq. (2) relates the output voltage V_{out} and its derivative V'_{out} to the metastable voltage γ_2. Since V'_{out} and I_{out} are directly related by (6), also the latter can be used for a good estimate of V_M. In detail, we can rewrite (2) as

$$V'_{out} = \frac{I_{out}}{C_L} = \frac{1}{\tau}(V_{out} - V_M). \quad (16)$$

```
.MODEL optMod1 OPT METHOD=BISECTION RELIN=1e-4
+ ITROPT=40
.PARAM outVal=optFunc1(vdd/2, vout_VL, vout_VH)
.DC vIn inVal inVal 1 SWEEP OPTIMIZE=optFunc1
+ RESULTS=optMeasure MODEL=optMod1
```

Listing 4. Bisection in *HSPICE*

Note that this is a linear function of the form $I_{out} = kV_{out} + d$, where the desired metastable value V_M can be expressed as

$$V_M = -\frac{\tau\, d}{C_L} = -\frac{d}{k}. \quad (17)$$

The values of k and d can be easily obtained by extracting several values of $I_{out}(V_{out})$ (e.g., by running `map`) and fitting a linear function. In this fashion, the metastable voltage V_M is derived extremely fast. Although this process has to be repeated for numerous choices of V_{in} to obtain γ_2, its execution time is still one of the lowest.

Similar to `expTran`, the method `expDC` can be run with traces towards *GND* as well as towards V_{DD}. As can be seen in Fig. 7, the difference between the values of $V_M^{\uparrow}$ and $V_M^{\downarrow}$ is much lower than for `expTran`. This improved accuracy seems to originate from avoiding the use of V'_{out}. For better results we again determine the intersection of the linear functions resulting from (17) for both directions.

D. Binary Search (`binary`)

A more pragmatic approach called `binary` sweeps V_{in} from V_L to V_H (cf. Fig. 1), and for each value V_{in} a binary search is performed to find a value of V_{out} such that I_{out} becomes zero. This bisection principle is also applied in [1], [18]. However, in contrast to the transient analyses used there, we again resort to determining I_{out} in the static case, cf. Section III-D. Since *DC* simulations are much faster to solve, the computation time can be reduced significantly.

To our advantage *HSPICE* has a built-in mechanism called *Bisection* to run a binary search. The corresponding code is shown in Listing 4. The first line states that we want to bisect, and at most 40 steps shall be carried out. Note that this narrows down the initial interval by a factor of 2^{40}. Most of the time, the algorithm finishes earlier, as the demanded accuracy (parameter *RELIN*) is reached first. In our case we demand that the difference between two consecutive values must be smaller than 0.01%. As can be verified in Fig. 4c, the residual error in V_M w.r.t. the analytical results (2) is indeed extremely small.

The third line sets the parameter *outVal* which determines the initial value of the output voltage V_{out} $(V_{DD}/2)$ and its sweep range. To ensure that the stable states are not contained in the latter, we set its boundaries to the last stable output values on γ_1 and γ_3. In the case of `opamp`, this corresponds to $\gamma_3(V_L)$ and $\gamma_1(V_H)$, respectively. The fourth line finally launches the *DC* analysis for the input voltage $V_{in} = inVal$ which means that this analysis has to be executed for each value of V_{in} separately.

E. DC Analysis (`static`)

In the course of our research we discovered that plain *DC* simulations on the unmodified implementation are already

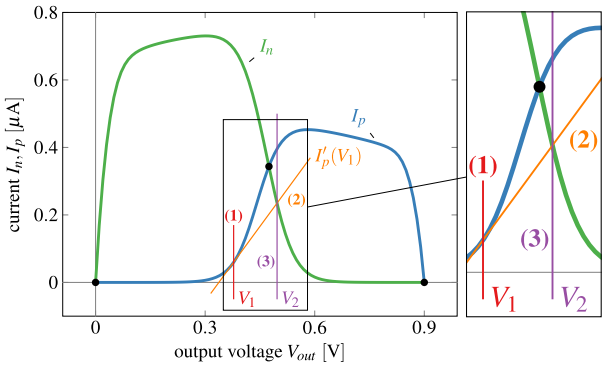


Fig. 8. Equilibrium output values V_{out} (•) determined by the *Newton-Raphson* algorithm for fixed V_{in}.

sufficient to determine the metastable values γ_2. We backtracked this feature to the operation principle of the *Newton-Raphson* algorithm that *HSPICE* utilizes to determine *DC* operating points in general [19]. To arrive at a stable operating point, the algorithm thrives to achieve $I_{out} = 0$ which is, as presented, a property of metastable states as well.

Fig. 8 depicts a showcase execution of the algorithm, where we assume a constant V_{in} and try to find a suitable V_{out}. Before the search starts, *HSPICE* sweeps V_{out} and records the current through the n- (I_n) and p-stack (I_p) of the gate driving the output. As expected the traces cross three times, i.e., for three values of V_{out} the currents exactly compensate, resulting in $I_{out} = 0$. While the outermost intersections mark the stable states of the S/T, the inner one represents the metastable state. The algorithm is started by an initial guess $V_{out} = V_1$ that can be provided by the user. The subsequent steps of the algorithm are (i) to determine the derivative of $I_p(V_1)$, (ii) to find the crossing point of the first-order approximation of $I_p(V_1)$ with I_n at $V_{out} = V_2$ and finally (iii) to restart the procedure with $V_{out} = V_2$, i.e., the value at the crossing point. The iteration stops when the voltage difference ΔV between two succeeding steps drops below a user-defined value.

Naturally, the initial guess determines which of the three crossings is approached. Thus, by starting close to γ_2, the algorithm will automatically converge to V_M. We have observed that a deviation of several tens of millivolts can be tolerated for the initial guess (even up to $V_{DD}/4$). Hence, connecting γ_1 and γ_3 by a straight line already provides suitable values.

The respective *HSPICE* code is shown in Listing 5. After setting the initial output value in line 2, the *DC* analysis is started in line 3 between $lowVal$ and $highVal$ with a step width of $stepWidth$. Since γ_2 is continuous, fast convergence and therefore low computing time is achieved by using the value found for the previous V_{in} as an initial guess (as it is done in *HSPICE*). For the circuit `opamp` (see Fig. 4c) the achieved accuracy is roughly 10^{-8} V. This rather high value can be retraced to the limited number of decimal places in the utilized output data format. If all other approaches are equally limited, their results are comparable.

V. Dynamic Metastability Behavior

Complementary to determining the static metastability values, we investigate in the following how the dynamic properties of an S/T implementation can be determined efficiently and accurately. Specifically, we are interested in the resolution time t_{res} and the corresponding time constant τ.

```
.PROBE DC V(out)
.NODESET out=outVal
.DC vIn lowVal highVal stepWidth
```

Listing 5. Executing `static` in *HSPICE*

A. Resolution Time Constant

The resolution time constant τ characterizes the exponential growth of a waveform resolving metastability and is thus a very important parameter. Implicitly, we have already utilized it in some of the methods presented in Section IV. The questions we address in the sequel are (i) whether the derived results are suitable to predict τ and (ii) if there exist other, overall simpler, methods to achieve this goal.

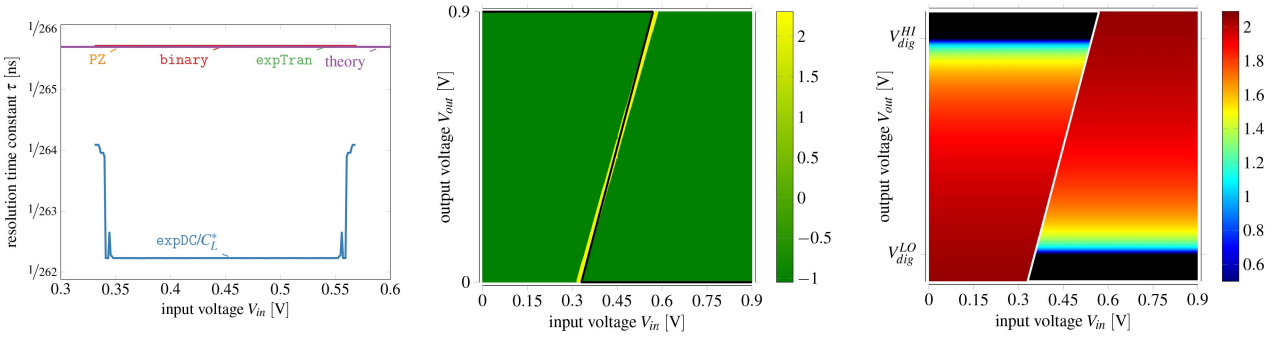
1) Method `expTran`: The straight forward approach, i.e., starting a transient simulation near the predicted metastable value V_M and fitting the resulting analog waveform, was implemented with `expTran`. In that approach, the resolution time constant τ was only calculated as a by-product since it was required in (14) to calculate the metastable voltage V_M.

For `opamp`, all points within one region share the same τ. It thus suffices to pick any segment of the resolution trajectory that does not cross region boundaries. Hence, any starting point close enough to γ_2 is suitable to compute the resolution time constant. In fact, the grid points obtained by `map` are already sufficient for this purpose. Fig. 9a reveals the perfect matches of τ compared to the analytic computation.

Unfortunately, state-of-the-art circuits, that will be discussed in Section VI, show slightly non-exponential resolution waveforms and thus variations in the resolution time constant within one Region. For comparison, we thus determined τ also in deep metastability by starting transient simulations in the metastable points delivered by the method `binary`. For `opamp` the differences are negligible, as can be seen in Fig. 9a.

2) Method `expDC`: τ is also computed as a by-product in `expDC`. In (16), the slope k of $I_{out}(V_{out})$ results to $k = C_L/\tau$. This relation allows a simple and accurate determination of τ, given that the output capacitance C_L is precisely known. Unfortunately, this is not the case for state-of-the-art circuits: In advanced CMOS technologies, C_L is constituted by gate capacitances, which change with bias and are subject to significant tolerances and noise. This makes it necessary to determine appropriate values of C_L based on transient simulations, which result in minor numerical inaccuracies. Thus, for `opamp` our results for the resolution time constant were already slightly off the theoretical values (cf. Fig. 9a). Furthermore, recall that the direct correspondence between I_{out} and V'_{out} was derived for a capacitor in Section III-C, so the relationship must be re-evaluated for systems with a dynamic order higher than 1.

3) Method `PZ`: An alternative approach, referred to as `PZ` (Pole-Zero), determines τ directly in the frequency domain, without resorting to *DC* or transient simulations. As shown in Section IV-A.4 for the method `control`, the linearized system dynamics captures all dynamic behavior in the transfer function $G(s)$, including the resolution time constant τ.



(a) resolution time constant τ (b) scaled responsiveness $f(V''_{out}/V'_{out})$ (c) resolution time $\log_{10}(t_{res}/t_0), t_0 = 1\,\text{ps}$

Fig. 9. Dynamic simulation results for `opamp`.

The transfer function $G(s)$ for the circuit `opamp` has the form (cf. (13)) $G(s) = \frac{1}{\tau s - 1}$. It can be seen clearly that the time constant is fully specified by the pole [17], whose value $\tau = 3.763\,\text{ps}$ for the circuit `opamp` is in perfect agreement with theory. In *HSPICE* we used the command *.pz* to automatically derive a list of all poles and zeros.

As we will show in Section VI, state-of-the-art circuits in general have multiple poles. Basically this makes their characterization using a (single) resolution time constant, as it is usually done in the context of metastability, questionable – since that implies a first-order dynamic behavior. Nevertheless, only considering the pole with the smallest positive real part, thus approximating the higher-order system with a first-order one, still delivers remarkably accurate results.

4) Application to Circuit `opamp`: To obtain a general understanding of the resolution behavior, we defined a regular grid in the plane, started a transient simulation with V_{out} close to the metastable value V_M and then determined for each grid point the respective slope of V'_{out} on a logarithmic scale, i.e., the responsiveness $r = \ln'(V'_{out}) = V''_{out}/V'_{out}$. The same figure of merit was already used by Reiher *et al.* [20] to describe the responsiveness of synchronizers. For exponential trajectories $r = 1/\tau$ is achieved. In realistic implementations we observe, however, variations of r, whereat very large positive and negative values in the V_{in}-V_{out} plane are encountered. In order (i) to scale all values by a factor A[3] and (ii) to remove non-interesting regions around the value 0 while preserving 0 itself we show the scaled responsiveness $f(r) = \text{sgn}(r)\log_{10}(|r/A|+1)$. Property (ii) is of specific interest as the value zero marks the boundary between resolving out of metastability and towards the final value, i.e., between Region 2 and 1 respectively 3. The results for `opamp` shown in Fig. 9b are in perfect agreement to the analytic calculations.

B. Resolution Time

The reasons to investigate the resolution time t_{res} are manifold: When analyzing metastability, especially in synchronous designs, the time to reach uniquely identifiable states is crucial. In a flip-flop, t_{res} merely depends on how deep the circuit is in the metastable state, i.e., how close to the real metastable point the resolution starts. In contrast, the situation is much more intricate for the S/T, since further parameters become relevant (even if we assume constant V_{in}). Firstly, the resolution in an S/T can start in any point on (or close to) γ_2. Depending on the actual choice, the circuit needs to overcome a specific voltage difference to reach the closest digitization threshold value V_{dig}^{HI} or V_{dig}^{LO} beyond which a clear logic `HI` or `LO` level, respectively, is detected.[4] Secondly, as we will see later in Section VI, the responsiveness r varies over the phase plane. Thus, the dynamics of the resolution process may significantly deviate between single values of V_{in}. In fact resolution trajectories that have to overcome a large voltage difference might reach the digitization threshold earlier than those starting much closer. Note that for a fair comparison a comparable distance to the metastable value has to be assured. This potentially counter-intuitive behavior is further investigated by computing the resolution time t_{res}.

In detail, t_{res} expresses the time it takes the output voltage V_{out} to reach the digitization threshold. It consists of t_{res}^S, which denotes the time spent in Region 1 and 3 before reaching V_{dig}^{HI} or V_{dig}^{LO}, respectively. It is potentially extended by t_{res}^M, which denotes the time for moving away from the metastable state inside Region 2. Using (3), we can formulate the output trajectory towards *GND* starting from an arbitrary value V_s within Region 3 $V_{out} = V_s exp(-t/\tau_3)$ as Reordering leads to a resolution time t_{res}^S for reaching V_{dig}^{LO} of

$$t_{res}^S = -\tau_3 \ln\left(\frac{V_{dig}^{LO}}{V_s}\right).$$

Analogously, for resolution towards V_{DD} (Region 1)

$$t_{res}^S = -\tau_1 \ln\left(\frac{V_{DD} - V_{dig}^{HI}}{V_{DD} - V_s}\right)$$

is obtained. For V_s within Region 2, t_{res}^S is constant and denotes the time span from reaching the boundary value between Region 2 and either 1 or 3, described by V_w, and the associated digitization threshold V_{dig}^{HI} or V_{dig}^{LO} respectively. The additional time it takes the circuit to move from V_s to V_w

[3]For our analyses we chose $A = r_{max}/200$ with r_{max} being the maximum value in the plane.

[4]Please note that V_{dig}^{HI} or V_{dig}^{LO} are thresholds at the *output* side, while V_L and V_H refer to the *input* side.

is denoted by t_{res}^M and can be derived by solving (2) as

$$t_{res}^M = \tau_2 \ln\left(\frac{V_w - V_M}{V_s - V_M}\right).$$

Based on the results from Section V-A, we computed for each grid point the time until the corresponding digitization threshold $V_{dig}^{HI} = 0.9\,V_{DD}$ or $V_{dig}^{LO} = 0.1\,V_{DD}$ is reached. For the example of `opamp`, the combined resolution time $t_{res} = t_{res}^M + t_{res}^S$ over the whole V_{in}-V_{out} plane is depicted in Fig. 9c. Although the used grid definitely hits the narrow Region 2, no significant increase in t_{res} can be observed there. The explanation is that close to the region border, the contribution of t_{res}^M to t_{res} is small. Starting halfway between γ_2 and the border to Region 1 or 3 results in $t_{res}^M = \tau_2 \ln(2)$ which evaluates in our case to $\approx 2.608\,\text{ps}$ – much less than t_{res}^S. To pronounce the discontinuity at V_M (since $t_{res}^M \to \infty$ for $V_s \to V_M$), we plotted the metastable values γ_2 in white.

VI. State-of-the-Art Circuits

Provided that an appropriate *SPICE* description of the circuit for each desired characterization method is available, the complete evaluation can be carried out without human interaction. Specifically for this reason we developed the *MEtastability Analysis Tool (MEAT)* which is publicly available.[5] In this section, we present the simulation results derived by this tool with the following aims:

a) aim I: We evaluate and compare the presented methods in a practical application. To this end, we apply all characterization methods to three different S/T implementations, as other circuits in literature are heavily based on these: a) the standard 6T implementation (`std`) b) an inverter loop (`loop`) [21] and c) an adjustable hysteresis type (`adjust`) [22]. For each circuit we determined the (meta-) stable states for 900 equally spaced values of V_{in}.

b) aim II: We investigate the behavioral differences among these implementations and also deviations from theoretical results [6]. Our circuits are analyzed as pre-layout circuits, i.e., without parasitics. This is reasonable since we investigate integrated components here and thus expect the parasitics (i) to be very small (compared to the gate capacitances) and (ii) to heavily depend on the actual layout.

As we do not have a precise theoretical model available that provides a ground truth for these implementations (like we had it for `opamp`), we need a different approach to verify the accuracy of the computed metastable values V_M^c. To this end, we start a transient simulation in each of them and then calculate the output deviation $\Delta = |V_{out}(t_0) - V_{out}(0)|$ at a fixed time $t_0 > 0$. Due to the strictly monotonic nature of the resolving trajectories, a higher Δ corresponds directly to a larger initial inaccuracy ϵ, i.e., $|V_M^c - V_M|$. Considering the exponential nature of the resolving waveform as shown in Section IV and using the resolution time constant τ (cf. Section V-A) allows us to compute $\epsilon = \Delta \,/\, \exp\left(\frac{t_0}{\tau}\right)$.

The fact that the feedback paths exhibit their own dynamics turns real circuits in good approximation into a second-order system. Consequently, the relation between I_{out} and V'_{out} becomes more complicated, which can, however, be modeled by a varying effective C_L^*. This correction is already considered in the results we present in the following.

[5] *https://github.com/jmaier0/meat*

A. Standard Implementation (`std`)

To compare our results against [1], we first analyze the implementation shown in Fig. 10a. The obtained (meta-)stable line (see Fig. 10b, γ_1 and γ_3 in solid red, γ_2 in solid orange) matches very well, which confirms that MEAT works as expected. In contrast to the analysis of Marino, γ_1 and γ_3 are neither constants, nor linear functions for this circuit. Instead, the stable values start to deviate from *GND* or V_{DD} when the respective threshold voltage is approached.

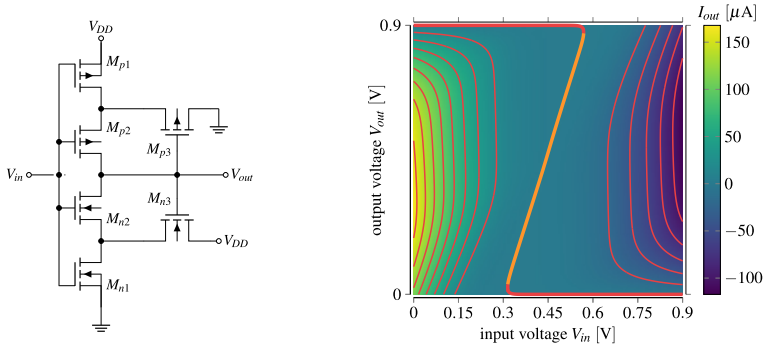
The heat map of the output current (see Fig. 10b), which utilizes linear spacing between the contour lines, reveals only moderate changes in I_{out} close to the metastable line. This can be expected from the exponential resolution trajectories predicted by theory. However, in contrast to the calculations of Marino [6], where V'_{out} only depends on the distance to the final, stable state (with horizontal contour lines, recall Fig. 4b), our results for the circuit `std` show mostly vertical contour lines, along with the maximum and minimum of I_{out} both located near $V_{DD}/2$. A resolution trajectory following a vertical (portion of the) contour line (which happens for constant V_{in}) exhibits a constant V'_{out} and hence a linear slope of V_{out} rather than an exponential curve.

Fig. 10c shows an accuracy comparison for the metastable voltage V_M: `binary`, which achieves a deviation of $\Delta \approx \pm 0.5\,\text{nV}$ after 200 ps, performs clearly the best. `expDC`, `static` and `control` are comparable and moderately precise, while `expTran` performs worst.

Finally Fig. 11a shows the resolution time constant τ determined using the methods `expTran`, `expDC`, `binary` and `PZ`. Their results match remarkably well. This plot shows τ over V_{in} assuming that all initial condition pairs (V_{in}, V_{out}) lie on γ_2 and consequently τ represents resolution from (almost) perfect metastability. It is apparent that, even within Region 2, the resolution time constant varies significantly over V_{in}. The smallest values can be found in the middle, around $V_{in} = 0.45\,\text{V}$. At the outskirts significantly worse values are observed meaning that these states are resolved slower.

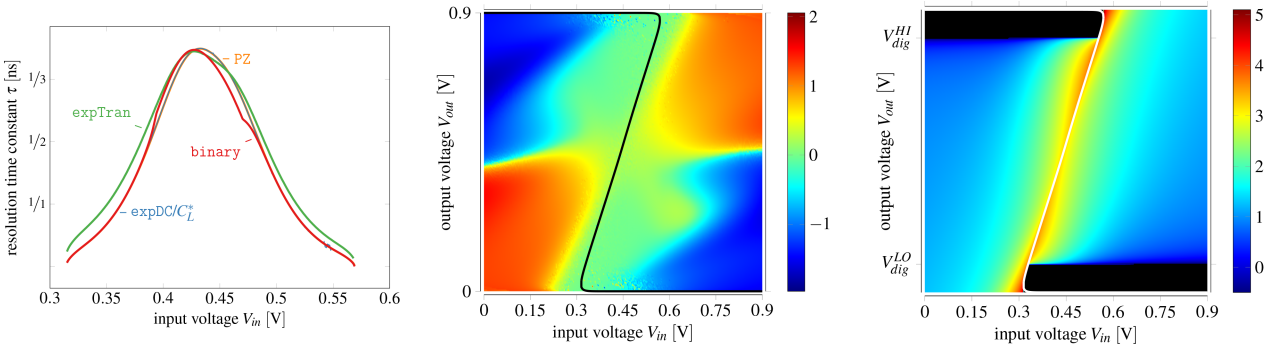
A more general view is given in Fig. 11b, which depicts the responsiveness r as a heat map in the whole V_{in}-V_{out} plane. The z-scaling is the same as for Fig. 9b, whereat in contrast to `opamp` significant variations are visible. In particular, grid points far away from the respective stable state tend to have positive values (red regions), while closer ones have negative ones (blue regions). Considering the usual switching behavior of real-world circuits, this makes perfect sense: The output trajectory for an arbitrary constant $V_{in} < V_L$ (vertical cut in the figure) shows in the first part an exponentially increase that turns into an exponential decay which asymptotically approaches V_{DD}. In both Regions 1 and 3, we observe relatively large absolute values which decrease when approaching γ_2 (and at the transition from increasing to decaying behavior). This contradicts Marino's results that predict a significantly larger resolution time constant τ for Regions 1 and 3 compared to Region 2 (cf. Fig. 9b). Obviously, the `opamp` model does not sufficiently match `std` in this respect.

Finally, the map of the resolution time t_{res} is shown in Fig. 11c. We observe, in comparison to `opamp` (cf. Fig. 9c), a further reaching and flatter dependence on the "horizontal" distance to the metastable value γ_2, but a similar clear



(a) transistor level implementation (b) I_{out} by `map` (c) output deviation Δ at $t_0 = 200\,\text{ps}$

Fig. 10. Metastability simulation results for `std`.



(a) resolution time constant τ (b) scaled responsiveness $f(V''_{out}/V'_{out})$ (c) resolution time $\log_{10}(t_{res}/t_0), t_0 = 1\,\text{ps}$

Fig. 11. Dynamic simulation results for `std`.

dependence on the "vertical" distance from the corresponding stable state. This indicates a weaker impact of the input on the overall S/T behavior. Remarkable is the fact that metastable values near $V_{in} = V_{DD}/2$ (assuming the same distance to V_M) resolve faster than values on the outskirts of γ_2, although the distance of V_M to the stable state might be shorter there.

B. Inverter Loop (`loop`)

The second circuit is a latch-like storage element (see the transistor level implementation in Fig. 12a). It consists of a pair of cross-coupled inverters, whereat the preceding logic is continuously connected via an input inverter. The hysteresis of the input/output behavior is defined by the ratio between the driving strength of the input inverter (transistors M_{p1} and M_{n1}) and that of the (weak) feedback inverter from the storage loop (M_{p2} and M_{n2}). For the latter we thus reduced the width to one tenth of their input counterparts.

The I_{out} map, see Fig. 12b, significantly differs from the one of `std`. Much like for `opamp` (Fig. 4b), the contour lines are horizontal at the border. Near γ_2, the current changes much more rapidly than for `std`, which also leads to lower values of the resolution time constant τ (one order of magnitude, see Fig. 13a), i.e., metastability is resolved much quicker. Interestingly, an increase in τ can be identified near $V_{DD}/2$. This may be due to the fact that in this region all transistors are saturated, meaning that voltage changes along the channel have little impact on the amount of conducted current. The methods `binary` and `PZ` once again deliver comparable results for τ. While `expTran` is only slightly off, `expDC` fails to deliver accurate values for this circuit. The main reasons are difficulties for the estimation of C_L^*.

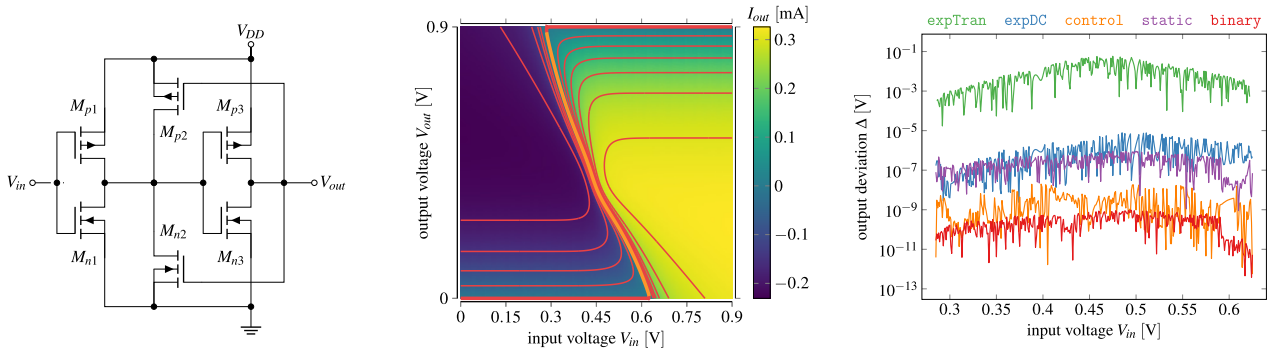
For this circuit, the metastable voltage V_M is computed most accurately by the method `binary` (see Fig. 12c), with `static` being very close and `expTran` performing significantly worse. Of special interest is `control` which occasionally outperforms `binary` in terms of accuracy.

The global view shown in Fig. 13b differs significantly from what we observed for `std`, cf. Fig. 11b. Outside the metastable region ($V_{in} < V_L$ and $V_{in} > V_H$) almost exclusively negative values are visible indicating the near-exponential behavior of V_{out} (highest derivative at start). Inside the hysteresis, lower values that further decrease near $V_{in} = 0.45\,\text{V}$, can be observed (cf. Fig. 13a). Note that the region boundary in Fig. 13b changes swiftly w.r.t. V_{in} near V_L and V_H. While inside the metastable region a slow and steady increase can be observed, rapid changes are observable outside of it.

The resolution time plot in Fig. 13c finally matches very well the already obtained results. The increased resolution time constant τ around $V_{in} = 0.45\,\text{V}$ results in a significant increase in the combined resolution time t_{res}.

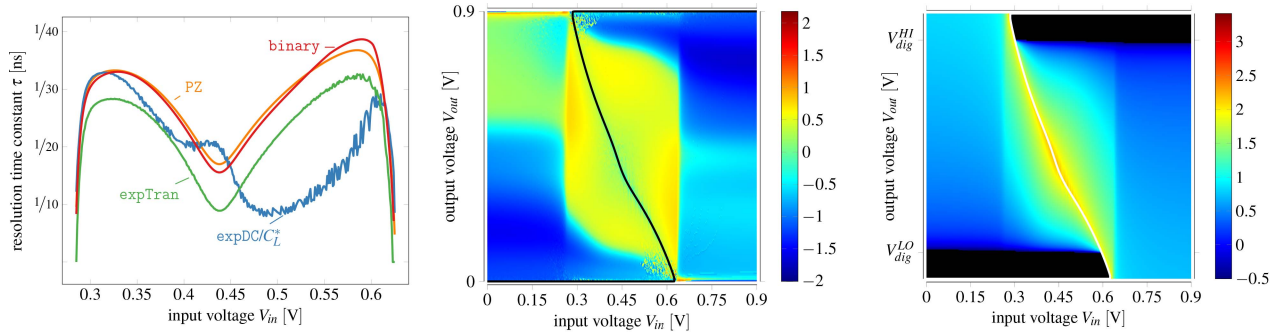
C. Adjustable Hysteresis (`adjust`)

In some applications it is important to adjust the hysteresis of the S/T during operation. One circuit that can be used for this purpose is called `adjust` and is shown in Fig. 14a. The additional input V_B alters the position and width of the



(a) transistor level implementation (b) I_{out} by `map` (c) output deviation Δ at $t_0 = 20\,\text{ps}$

Fig. 12. Metastability simulation results for `loop`.



(a) resolution time constant τ (b) scaled responsiveness $f(V''_{out}/V'_{out})$ (c) resolution time $\log_{10}(t_{res}/t_0), t_0 = 1\,\text{ps}$

Fig. 13. Dynamic simulation results for `loop`.

hysteresis. In our simulations we used $V_B = V_{DD}$ as in this case the hysteresis is the widest and thus the circuit has the largest amount of metastable states.

The first remarkable aspect to be observed in Fig. 14b is the vertical section of γ_3 with its relatively large peak value of V_{out}. It reaches up to about 0.3 V which is one third of the supply voltage and almost certainly in the forbidden region, i.e., above V_{dig}^{LO}. Those states can be easily reached by a V_{in}-ramp stopping at a defined value, which implies low resilience against metastability. The `map` in Fig. 14b shows similarities to that of `std` (cf. Fig. 10b), especially in the right half. In the left half, the vertical contour lines are even more pronounced.

Due to the high similarity to `std` on the transistor level the achieved results for accuracy levels, the (initial) resolution time constant τ and the resolution time characteristics are very much related and thus not explicitly shown here. Note that in absolute terms, the circuit `adjust` exhibits the largest peak value for the resolution time constant τ. This also becomes apparent in the global map shown in Fig. 14c, where the large green area indicates slow changes.

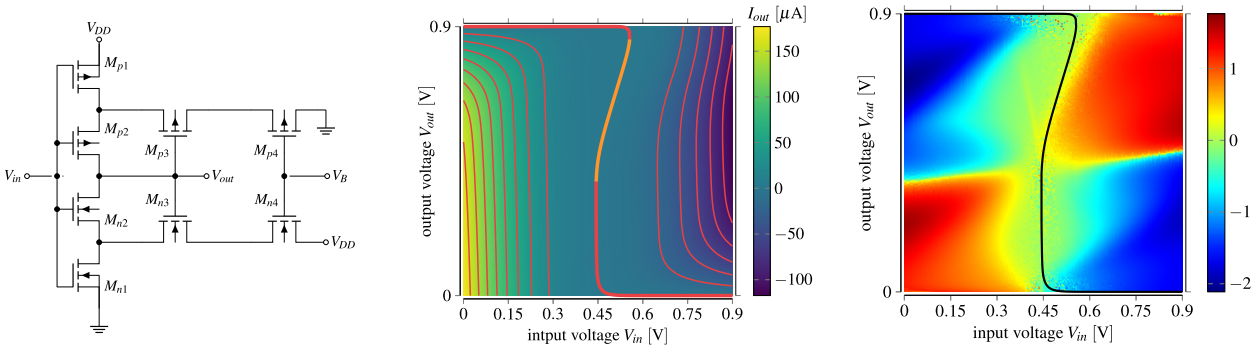
VII. Comparison & Evaluation

In this section, the experiences gained throughout the characterization of three real-world S/T implementations are utilized for comparing and evaluating the methods that have been introduced in Sections III, IV and V. Naturally, our main criteria for this evaluation are accuracy, resolution, ease of use, computing time and scalability.

The difficulty in doing an objective comparison is that trade-offs between these parameters are possible. For example, the accuracy can often be increased by investing more computing time. Similarly, the grid resolution of all presented methods can be made arbitrarily high. In practice, however, limitations apply such as the finite simulator precision (internal number format), the required computing time and the available output file formats. The latter raised significant issues for `expDC` as we only managed to export results with 7 positions after the decimal point from *HSPICE*, while for all other methods 10 positions were possible. Due to the above reasons, we restrict ourselves to qualitative analyses in this work. Nevertheless, to allow for a quantitative classification of the evaluated methods, Table I lists the computing times required to obtain the results that were presented in this paper on our machine (Intel Xeon X5650, 1600 MHz, 32 GB RAM, CentOS 6.10). Note that the hysteresis and therefore the number of metastable grid points between V_L and V_H differ among the S/T implementations.

c) `hyst`: Using the method `hyst` the hysteresis curve is determined by two *DC* analyses starting at $V_{in} = GND$ and $V_{in} = V_{DD}$, respectively. Due to the fact that γ_1 and γ_3 are almost constant, their exact characterization is simple and fast. The accuracy is directly dependent on the simulation tool and the circuit element model, and is therefore excellent, since no assumptions (e.g., on signal shapes) apply.

For obtaining V_L and V_H with high resolution, as well as exploring the non-ideal shape of γ_1 and γ_3 in the proximity



(a) transistor level implementation (b) I_{out} by `map` (c) scaled responsiveness $f(V''_{out}/V'_{out})$

Fig. 14. Simulation results for `adjust`.

of these threshold voltages, a small step size is desirable. Fortunately, the computation time scales only linearly with the number of samples. Consequently, state-of-the-art designs can be processed with excellent resolution within several seconds.

d) `map`: Similar statements as for the method `hyst` can be made for the phase diagram `map`. The significant difference, however, is that the grid is now two-dimensional (V_{in} and V_{out}), and therefore an increase of the resolution has a quadratic impact on the computing time. In this paper we used a regular grid in the whole V_{in}-V_{out} plane, but much smarter choices are conceivable. The effort could, for example, be massively reduced if the grid was continuously refined with decreasing distance to γ_2.

Using I_{out} as an indirect measure for V'_{out}, reduces on the one hand the computing time significantly. On the other hand, however, the accuracy suffers due to uncertainties associated with C_L^*, as outlined in Section VI-A. Consequently the contour lines obtained using the method `map` should be considered as a qualitative result only – which is, nevertheless, often sufficient. If accurate quantitative results are required, the overhead of directly determining V'_{out} must be accepted.

e) `expTran`: While other approaches purely rely on the data points derived from analog simulations, `expTran` incorporates analytic considerations as well. In fact, a few values extracted from the simulation are used to parameterize a known (namely exponential) function. The latter then allows to quickly derive τ and V_M with a resolution that may be significantly better than that of the simulation tool. This property makes `expTran` appealing.

However, our results show that it achieves the worst accuracy for the metastable values γ_2, and quite some deviations for the resolution time constant τ. The reasons for these imperfections are (i) the relatively poor accuracy of *HSPICE* for determining V'_{out}, and (ii) the fact that in real-world circuits the resolution trajectories are not perfect exponential functions, even in Region 2. In detail, we have observed that V'_{out} changes more rapidly than an exponential function in the vicinity of the region boundaries. At the same time, care must be taken that the data points are extracted from within Region 2 (recall, it may be very small), as the trajectory definitely follows a different function outside. Therefore, the method `expTran` is more challenging to apply.

For each value of V_{in} within the hysteresis, two transient simulations are carried out. Since the initial values are taken from `map`, a finer grid of `map` also improves the accuracy of `expTran`. However, as denoted before, the computation time scales quadratically for `map`.

f) `expDC`: This method is very similar to `expTran`, as also the grid points of `map` closest to γ_2 are utilized. In contrast, however, no separate simulations are required to predict the metastable voltage, which enables a rather quick execution, typically within a few seconds. Unfortunately, it is necessary to determine the implicit load capacitance C_L^* in advance, whereat its value varies among operating points and thus requires transient simulations and proper averaging.

Similar to `expTran`, the method `expDC` also has the potential to speed up the simulation by leveraging the knowledge of the resolution trajectories being exponential, but then suffers in accuracy when this assumption is not perfectly met by the circuit. Still, for trajectories originating from γ_2, the results prove to be very accurate.

The resolution time constant τ is extracted from (17) and the comparison between static and dynamic output current. Although this is easily possible, the challenges regarding C_L^* described above and fitting to numerically noisy simulation data, sometimes lead to rather poor results. Consequently, for predicting τ, `expDC` is, on its own, only of limited use.

g) `binary`: For each value of V_{in} within the hysteresis a binary search has to be executed. While the overall amount of simulations thus scales with the grid granularity of V_{in}, the amount of binary steps has hardly any impact on the computation time. We experienced a reduction by only 10 % when lowering the number of iterations from 40 to 20 whereas the accuracy was degraded by four orders of magnitude. The results achieved for V_M are among the most accurate ones, however, τ cannot be directly computed using this approach.

h) `control`: The approach `control` essentially relies on a controller that stabilizes the dynamic system, i.e., the S/T, in a metastable state. Naturally, the parametrization of that controller significantly influences how fast and accurate V_M will be approached: With a slow controller, convergence will be unproblematic and robust, while a fast controller introduces overshoot, ringing and eventually even instabilities. That is why the choice of the controller gain K is critical. Although, theoretically, the metastable voltage V_M can be approached perfectly accurate, it would take an infinite amount of time to do so. For this reason, and also due to the limited accuracy of *SPICE*, we settled for a simulation time in which the controlled circuit approximately reaches a steady state. In this fashion, very accurate results could be achieved. Fortunately

TABLE I
OVERVIEW OF COMPUTING TIMES

	computing time [s]		
circuit	`std`	`loop`	`adjust`
metastable grid points	282	378	125
`hyst`	1.817	2.297	1.842
`binary`	238.834	370.135	115.272
`map`	661.302	676.525	797.702
`control`	3581.520	2340.700	3258.726
`expTran`	841.718	1089.741	334.582
`expDC`	791.997	890.129	340.751
`static`	2.572	2.818	2.627
τ (`binary`)	1194.648	552.158	537.934
`PZ`	730.889	1064.792	241.888
t_{res} and V''_{out}/V'_{out}	14 102.607	3939.382	11 228.703

it is possible to decrease the accuracy of the simulation to enlarge the simulation time horizon that can be processed with the same computational effort, while in turn improving the accuracy of the obtained metastable value V_M.

With our analysis in the frequency domain, we explored how a simple controller design for a proportional controller might be performed. Certainly, control theory offers techniques for further improvement. Simply guessing the controller gain K did not work in our analyses, while its systematic determination entails an *AC* analysis plus a suitable investigation of the resulting poles and zeros. Experiments with all S/T implementations in this work have shown that the necessary stability condition for the closed-loop system (8) already provides a very good approximation for the stability boundaries. The accuracy lies below 0.1% also for higher-order systems with $N > 2$. Hence, in practice, the additional stability conditions originating from the Hurwitz test can be neglected.

Overall, this approach, while being elegant in exposing the metastable value V_M for direct extraction, turns out to be rather time consuming. We primarily see its application in cases where little to no information about the metastable behavior or the circuit itself is available.

i) `static`: The fact that the *DC* analysis in *HSPICE* reuses a preceding stable configuration as starting point for the succeeding iteration, makes this type of simulation very fast and accurate. In general, results can be obtained within a couple of seconds. The biggest problem we faced is the limited output data format, which reduced the achievable (exportable) precision significantly.

Essentially, the approach `static` heavily relies on the *Newton-Raphson* algorithm that *HSPICE* uses internally for static analyses. This means that any future changes in the internals of *HSPICE* may invalidate the method, although we are optimistic that this will not be the case. Furthermore the resolution time constant τ cannot be estimated.

j) `PZ`: Determining the resolution time constant τ based on the smallest positive pole of the circuit works remarkably well, even in the presence of multiple poles. Clearly, one has to run an *AC* analysis in advance to extract the respective data. This has to be done for each value of V_{in} with the initial condition $V_{out} = V_M$, so the computational effort increases linearly for finer granularity.

k) Responsiveness r and Resolution Time t_{res}: The heat maps for r and t_{res} are the result of two transient simulations per value of V_{in}. Although the simulation time is kept short using a simple heuristic, starting in deep metastability with low driving strength leads to a significant computational effort and consequently long run time. In this case not only the computation time of *HSPICE* has to be considered; the extraction of r and t_{res} from the plain simulation traces also creates non-negligible computational efforts.

l) General Observations: While using both transient and *DC* analyses, overall we experienced that the former are much harder to handle. The reason is that more parameters have to be defined, most notably the time period of the simulation. In addition further complications, such as extracting a specific part of the simulation in `expTran` or finding an appropriate controller gain K for `control`, have to be overcome. In total, *DC* analyses achieve better results with less computation time and simpler methods. In this regard frequency domain analyses, e.g., determining poles and zeros, are comparable to *DC* since they are also easy to apply.

Finally we want to emphasize that the proposed methods are not restricted to S/Ts. We verified this by exemplarily running `static` and `control` on a latch formed by a loop of asymmetric inverters (width ratio $1/10$) separated by a transmission gate. In both cases the metastable configuration was quickly achieved, which indicates a potential general applicability of our analyses and thus a large application area.

m) Validity of the simulation approach: Simulating metastability pushes transistor models and simulation engine towards their limits. To rule out the introduction of potential artifacts, we have taken great care to verify our results. In particular, the comparison with the known-correct theoretical results for `opamp`, as well as the comparison of the results delivered by the diverse methods (that leverage different features of the simulation engine) already provide some certainty. In addition, experimental results in [11], [12] largely confirm the validity of simulation results for S/T metastability.

Furthermore, the bundle of diverse methods we presented in this paper allows the reader to double-check own results obtained with one specific method by using another.

VIII. CONCLUSION AND FUTURE WORK

In this paper we presented a guide towards a better understanding of the Schmitt-Trigger (S/T). To this end we introduce and evaluate several approaches to comprehensively characterize the metastable behavior. Based on various simulation methods, (i) the (meta)stable states, (ii) the rate of change in the whole V_{in}-V_{out} plane as well as (iii) the dynamic behavior in the form of the resolution time constant, the responsiveness and the total resolution time are covered. Comparisons to analytic calculations of an ideal OpAmp implementation allow us to quantify the fundamental accuracy limits of the investigated methods. The application to three state-of-the-art CMOS circuits shows the feasibility of our approaches whereat methods based on static considerations deliver results faster and with higher precision. Finally, all proposed methods have been included in the publicly available tool MEAT which makes them, in our opinion, a viable resource for simple and fast metastability characterization of an S/T implementation. Even more, first results indicate that also circuits beyond the Schmitt-Trigger can be efficiently analyzed.

The S/T has only recently been considered in metastability analysis. Future work will thus be devoted to closing the gap to

other circuit elements like the latch, for example to derive an expression for estimating the reliability impact of metastable upsets, comparable to the MTBU formula in flip-flops. This, however, requires to take the (possibly changing) input into account as well which increases the complexity significantly.

The deviating behaviors of the investigated S/T implementations also raise the question, which one performs better in specific situations and what the responsible properties are. Based on our results, we are confident to either systematically (i) develop highly optimized circuits, or at least (ii) improve existing ones, e.g., by proper transistor scaling in the future.

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